CLAIMS

Having thus described our invention in detail, what we claim is new and desire to secure by the Letters Patent is:

1. A method of fabricating a semiconductor device comprising the steps of:

(a) providing a collector having a first doping type, said collector comprising a sub-collector and a diffusion;

(b) providing the diffusion over said sub-collector, said diffusion having said first doping type;

(c) forming a base;

(d) forming an emitter; and

wherein said diffusion has a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage and a doping sufficiently high to restrict base widening when the base-emitter junction is forward biased.

2. The method of Claim 1 wherein in said providing step (b) said vertical width of said diffusion is less than about 2000 Å.

3. The method of Claim 2 wherein in said providing step (b) said vertical width of said diffusion is from about 800 to about 1200 Å.

4. The method of Claim 1 wherein in said providing step (b) said diffusion has a peak doping concentration and said collector has a peak doping concentration, wherein said peak doping concentration of said diffusion is greater than said peak doping concentration of said collector.

5. The method of Claim 1 wherein in said providing step (c) said base has a peak doping concentration and wherein said diffusion has a peak doping concentration that is lower than said peak doping concentration of said base.

6. The method of Claim 1 wherein in said providing step (b) said diffusion comprises a dopant selected from the group consisting of As, Sb and P.

7. The method of Claim 6 wherein said dopant is Sb.

8. The method of Claim 6 wherein in said providing step (b) said diffusion is formed by ion implantation and activation annealing.

9. The method of Claim 8 wherein said ion implantation is performed at an ion dose of from about 2E11 to about 1E13 cm^{-2} and at an energy of from about 20 to about 150 keV.

10. The method of Claim 9 wherein said ion implantation is performed at an ion dose of from about 5E11 to about 5E12 cm^{-2} and at an energy of from about 30 to about 50 keV.

11. The method of Claim 8 wherein said activation annealing is performed at a temperature of about 900°C or higher for about 15 seconds or less.

12. The method of Claim 1 wherein in said forming step (c) said diffusion is located adjacent the base-collector junction.

13. The method of Claim 1 wherein in said forming step (c) further comprises providing a lightly doped collector separating said diffusion from said base.

14. The method of Claim 13 wherein in said forming step (c) said lightly doped collector has a vertical width of about 1000 to about 3000 Å.

15. The method of Claim 1 wherein said forming step (c) comprises forming a heterojunction.

16. The method of Claim 15 wherein in said step of forming a heterojunction comprises depositing a SiGe-containing layer on said collector, said SiGe-containing layer comprising a polycrystalline region abutting a single-crystal region.

17. The method of Claim 16 wherein said forming step (d) includes forming a patterned insulator on said SiGe-containing layer, wherein said patterned insulator includes an opening that exposes a portion of said single-crystal region, and forming an emitter polysilicon on said patterned insulator and in said opening.

18. The method of Claim 17 wherein said step of forming a patterned insulator on said SiGe-containing layer comprises lithography and etching.

19. The method of Claim 16 wherein portions of said single-crystal region are doped so as to form extrinsic base regions therein.

20. The method of Claim 16 wherein said SiGe-containing layer comprises SiGeC.

21. The method of Claim 16 wherein said step of depositing a SiGe-containing layer is performed using a low-temperature deposition process selected from the group consisting of chemical vapor deposition (CVD), plasma-assisted CVD, atomic layer deposition (ALD), chemical solution deposition and ultra-high vacuum CVD.

22. The method of Claim 21 wherein said collector includes a deep collector that is formed by ion implantation and annealing.

23. The method of Claim 1 wherein in said providing step (a) said sub-collector is formed by ion implantation into a substrate or by epitaxially growing said sub-collector on a substrate.

24. A bipolar transistor comprising:

an emitter, a base, a collector, a base-emitter junction, and a base-collector junction, wherein said collector comprises a sub-collector and a diffusion between said sub-collector and said base-collector junction, wherein said diffusion has a vertical width sufficiently narrow to avoid lowering collector-base breakdown voltage and a doping sufficiently high to restrict base widening when the base-emitter junction is forward biased.

25. The bipolar transistor of Claim 24 wherein said diffusion is located adjacent the base-collector junction.

26. The bipolar transistor of Claim 24 wherein said vertical width of said diffusion is less than about 2000 Å.

27. The bipolar transistor of Claim 26 wherein said vertical width of said diffusion is from about 800 to about 1200 Å.

28. The bipolar transistor of Claim 24 wherein said diffusion has a peak doping concentration and said collector has a peak doping concentration, wherein said peak doping concentration of said diffusion is greater than said peak doping concentration of said collector.

29. The bipolar transistor of Claim 24 wherein said base has a peak doping concentration and wherein said diffusion has a peak doping concentration that is lower than said peak doping concentration of said base.

30. The bipolar transistor of Claim 24 wherein said diffusion comprises a dopant selected from the group consisting of As, Sb and P.

31. The bipolar transistor of Claim 30 wherein said dopant is Sb.

32. The bipolar transistor of Claim 24 further comprising a lightly doped collector separating said diffusion from said base.

33. The bipolar transistor of Claim 32 wherein said lightly doped collector has a vertical width of about 1000 to about 3000 Å.

34. The bipolar transistor of Claim 24 wherein said diffusion provides a higher speed of the transistor by restricting base widening.

35. The bipolar transistor of Claim 24 wherein said sub-collector is on a semiconductor substrate.

36. The bipolar transistor of Claim 35 wherein said semiconductor substrate is a semiconducting material selected from the group consisting of Si, Ge, SiGe, GaAs, InAs, InP, Si/Si, Si/SiGe and silicon-on-insulators.

37. The bipolar transistor of Claim 24 wherein said diffusion has a dopant concentration of from about 5E16 to about 5E17 cm^{-3}.

38. The bipolar transistor of Claim 24 wherein said diffusion has a dopant concentration of from about 8E16 to about 2E17 cm^{-3}.

39. The bipolar transistor of Claim 24 wherein the transistor comprises a heterojunction.

40. The bipolar transistor of Claim 39 wherein said heterojunction comprises a SiGe-containing base layer on a silicon substrate.

41. The bipolar transistor of Claim 40 wherein said SiGe-containing base layer comprises a polycrystalline region abutting a single-crystal region.

42. The bipolar transistor of Claim 41, wherein said emitter comprises polycrystalline silicon contacting a portion of said single-crystal region through an opening in a patterned insulator.

43. The bipolar transistor of Claim 41 wherein said single-crystal region includes extrinsic and intrinsic base regions.

44. The bipolar transistor of Claim 40 wherein said SiGe-containing base layer comprises SiGeC.